(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 420 672 A1**

# (12) EUROPEAN PATENT APPLICATION

(21) Application number: **90310645.8**

(51) Int. Cl.5: **H01L 21/761**

(22) Date of filing: **28.09.90**

(30) Priority: **29.09.89 JP 254942/89**
**28.12.89 JP 344316/89**

(43) Date of publication of application:
**03.04.91 Bulletin 91/14**

(84) Designated Contracting States:
**DE IT**

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## (54) Semiconducteur stubstrate structure for use in power IC device.

(57) A wafer substrate structure has a P type epitaxial wafer layer (21). An N+ type region separation layer (22) is formed in the wafer layer (21) to define a first closed region (A) and a second region (B) neighboring thereto. Formed in the first region (A) are a P- type layer (23) and an N- type layer (24) stacked thereon and serving as a high-resistance layer for forming the first element. An N- type layer (24) serving as a high-resistance layer exists in the second region (B) of the wafer layer (21). These high-resistance layers are defined by separating a single semiconductor layer (24) by an N+ type diffused separation layer (26). Forming a high-voltage transistor as a power element in the first region to be PN junction-separated brings a "double PN junction separation" structure wherein the first region (A) is electrically separated by PN junction from the second region (B) and the high-voltage transistor is also PN junction-separated in the first region (A).

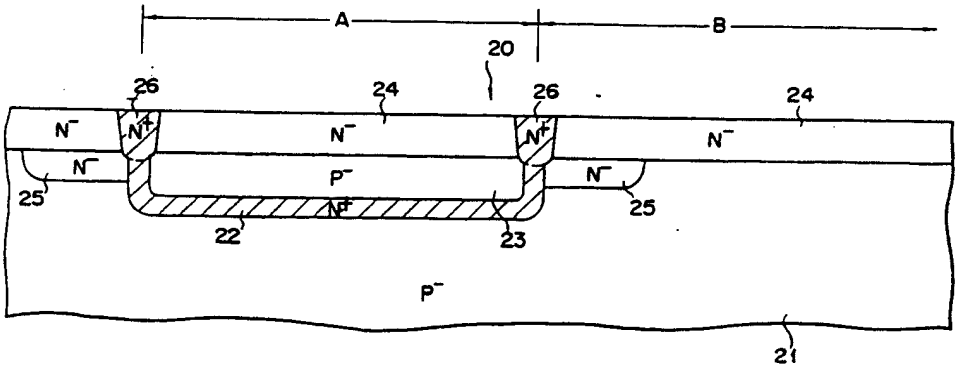


FIG. 1

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# SEMICONDUCTOR SUBSTRATE STRUCTURE FOR USE IN POWER IC DEVICE

The present invention relates to semiconductor devices and, more particularly, to a semiconductor wafer suitable for integration of a circuit arrangement for power IC devices which include high-voltage transistors.

Power semiconductor devices, such as bipolar transistors and metal-oxide semiconductor field effect transistors (MOSFETs), are generally connected in series with each other in an inverter circuit or the like. In such a circuit, diodes are often connected in parallel with series-connected transistors, respectively. In fact, many semiconductor IC manufacturers have produced circuit modules in which transistors connected in series with each other in this manner and diodes connected in parallel therewith are packaged into a single chip.

One of circuits using such circuit modules is a three-phase inverter circuit, which includes the above-mentioned series-transistor/parallel diode circuit module and gate circuits for driving and controlling the module. Typically, such an inverter circuit includes three sets of series-circuits of transistors, each set consisting of a couple of bipolar transistors that are connected in series with each other. Six diodes are respectively connected in parallel with these bipolar transistors. Each of these transistors is provided with a gate circuit for driving it. The three sets of transistor circuits have two common connection terminals, one of which serves of which acts as a ground terminal.

With such an arrangement, when the six gate circuits are to be integrated together onto one chip, optimal regions separation cannot be performed due to the difference in electrical operating environment among different gate circuit modules on the same wafer substrate. This problem is a serious factor which delays realizing IC packaging of high-voltage circuits for power semiconductor devices, which have been strongly demanded for a long time. The difference in electrical operating environment may be caused in a case wherein a certain one of gate circuits having the same element structure is constantly biased by a higher voltage, or a case wherein the reference voltage to a specific one of gate circuits greatly varies within the range of a power source voltage to a ground potential depending on the operating states of another adjacent circuit.

Presently available dielectric isolation techniques may be used to perform the "individual independence regions separation" on the same wafer substrate, i.e., in order to electrically separate a certain gate circuit module region from the remaining ones so as to allow it to operate independently of the operating states of the remaining ones. However, a wafer substrate having the dielectric separation structure suffers from several drawbacks, i.e., a complicated manufacturing process, limited integration, and high cost. These drawbacks make semiconductor manufacturers hesitate to apply the dielectric separation structure to the integration of high-voltage transistors and peripheral circuits therefor. If different operating environments of the respective gate circuits are compensated by techniques in circuit design, an overall circuit arrangement is undesirably complicated.

It is therefore an object of the present invention to provide a new and improved technique for separating elements-formation regions of a semiconductor wafer.

It is another object of the invention to provide a new and improved semiconductor wafer structure which is excellent in element separation characteristics and hence can be suitably applied to power semiconductor ICs.

In accordance with the above objects, the present invention is addressed to a specific substrate structure which includes a semiconductive substrate having a PN junction layer, and a closed region formed on the substrate and separated from other portions of the substrate by PN junction-separation. The closed region has a PN junction substrate. The closed region serves as an elements-formation region allowing the formation of a semiconductor active element such as a high-voltage transistor which is subjected to PN junction-separation therein. With such "double PN junction separation" structure, the above objects can be achieved. The "double PN junction separation" structure can be satisfactorily manufactured by using a presently available manufacturing process.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Figure 1 is a diagram schematically showing a sectional structure in a main part of an epitaxial semiconductor wafer according to a preferred embodiment of the present invention;

Figures 2A to 2D are diagrams schematically showing sectional structures obtained in main steps of a manufacturing process for the wafer in Figure 1;

Figure 3 is a diagram schematically showing a sectional structure in a main part a device obtained by integrally forming transistors in

elements-formation regions of the wafer in Figure 1;

Figure 4 is a diagram showing an electrically equivalent circuit of the device in Figure 3;

Figure 5 is a diagram schematically showing a sectional structure in a main part of an epitaxial semiconductor wafer according to the second embodiment of the present invention;

Figure 6 is a diagram schematically showing a sectional structure in a main part of an epitaxial semiconductor wafer according to the third embodiment of the present invention;

Figure 7 is a diagram schematically showing a sectional structure in a main part of an epitaxial semiconductor wafer according to the fourth embodiment of the present invention;

Figures 8A to 8E are diagrams schematically showing sectional structures obtained in main steps of a manufacturing process for the wafer in Figure 7;

Figures 9A and 9B are diagrams showing a sectional structure of IC devices obtained by integrally forming a plurality of transistors in elements-formation regions of the epitaxial wafer in Figure 7;

Figure 10 is a diagram schematically showing a sectional structure in a main part of an epitaxial semiconductor wafer according to the fifth embodiment of the present invention;

Figures 11A to 11D are diagrams schematically showing sectional structures obtained in main steps of a manufacturing process for the wafer in Figure 10;

Figure 12 is a diagram showing a sectional structure of a sample of an IC structure to which the wafer in Figure 10 is employed; and

Figure 13 is a diagram showing a sectional structure of another sample of an IC structure to which the wafer in Figure 10 is employed.

Referring now to Figure 1, an epitaxial semiconductor wafer in accordance with one preferred embodiment of this invention is designated generally by reference numeral "20." The semiconductor wafer 20 has of a lightly-doped P conductivity type (to be refereed to as a "P- type" hereinafter) silicon substrate 21. The substrate 21 has a first region A in which a plurality of elements electrically separated from each other by PN junction-separation are to be formed, and a second region B positioned outside the region A. The second region B is also a region in which a plurality of elements electrically separated from each other by PN junction-separation are to be formed.

In the first region A, a heavily-doped N type (N+ type) buried layer 22 is formed by diffusion in the P-type substrate 21. A P- type semiconductor layer 23 is formed by epitaxial growth in the N+ type diffusion layer 22. This epitaxial layer 23 has substantially the same order of impurity concentration as that of the substrate 21. A lightly-doped N type (N- type) shallow semiconductor layer 24 is formed by epitaxial growth on the entire top surface of the substrate 21 throughout the regions A and B. The semiconductor layer 24 serves as a high-resistance layer.

A shallow N- type semiconductor layer 25 called a "reduced surface field layer," or the "RESURF layer" for short, is formed under the high-resistance layer 24 in the substrate 21 so as to surround the N+ type diffusion layer 22. An N+ type semiconductor layer 26 is formed in the high-resistance layer 24, as a low-resistance layer, so as to correspond to the planar shape of the N+ type region of the diffusion layer 22. The low-resistance layer 26 is larger in depth than the high-resistance layer 24; therefore, the low-resistance layer 26 penetrates the high-resistance layer 24 and is electrically connected to the underlying layer 22, whereby the potential of the diffusion layer 22 is "exposed" on the top surface of the substrate 21.

With such an epitaxial wafer 20, both the first region A and the second region B can have "N-/P-" structures. This enables a plurality of elements to be successfully formed in each of the first and second regions A and B in accordance with a normal PN junction-separation technique.

According to this embodiment, individual one of the elements that are integrated on the wafer can be successfully separated by PN junction-separation from the other elements. In addition, a "double PN junction-separation" structure is obtained in which circuit regions each having plural types of elements are separated from each other by PN junction separation. Since such a wafer structure allows each circuit region to be freely set in a desired different potential independently of the remaining regions, the wafer structure is especially suitable for integration of high-voltage transistors and their peripheral circuits.

A method of manufacturing the epitaxial semiconductor wafer 20 will be described below with reference to Figures 2A through 2D. A P- type silicon substrate 11 is prepared. A groove 31 having a preselected depth is formed in the first region of the substrate 21 using a silicon etching technology, such as a reactive ion etching method. An N+ type diffusion layer 22 of high-impurity concentration is formed in the inner surface of the groove 31, as shown in Figure 2A.

Subsequently, as shown in Figure 2B, a P- type epitaxial-growth layer 23 is formed on the overall top surface of the resultant layer structure. The wafer surface is then subjected to a lapping treatment so that the wafer surface is flattened to leave the P- type epitaxial-growth layer 23 in only the groove 31 as shown in Figure 2C. An N- type

layer 25 serving as a RESURF layer is formed on the flat top surface section of the substrate 21.

Thereafter, as shown in Figure 2D, an N- type epitaxial-growth layer 24 is formed on the resultant wafer substrate 21. Finally, an N+ type diffusion layer 26 is formed.

Figure 3 shows an IC structure which is obtained by integrally forming a plurality transistors in first and second regions A and B of the above-mentioned epitaxial semiconductor wafer 20. In Figure 3, of transistors formed in each of the regions A and B, only one transistor Ql is visible in the region A, while only one transistor Q2 is visible in the region B.

As shown in Figure 3, collector buried layers 41a and 41b, which are omitted in the previous wafer structure shown in Figure 1, are respectively formed in the elements-formation regions A and B, before the formation of an epitaxial layer 24. Each elements-formation region is PN junction-separated, i.e., electrically separated by PN junction, from the remaining part of the wafer structure by P+ type layer 42a or 42b. In the region A, a base layer 43a, an N+ type emitter layer 44a, an N+ type collector layer 44a, anu an N+ type collector voltage take-out layer 45a are formed, thereby constituting the transistor Q1. In the other region B, a base layer 43b, an N+ type emitter layer 44b, an N+ type collector layer 44b, and an N+ type collector voltage take-out layer 45b are formed so as to constitute the transistor Q2.

Transistor circuits in the first and second regions A and B constitute gate circuits G1 and G2, respectively in an equivalent circuit diagram as in Figure 4. Therefore, a terminal P1, which connects in common the P+ type separation layer 42a in the first region A to the N+ type layers 22 and 26 for separating the layer A from the layer B, acts as a reference voltage terminal the voltage potential of which changes within a range defined between 0 volts and a power source voltage Vcc. A terminal P2 that is connected to the P+ type separation layer 42b in the second region B functions as a fixed ground potential terminal.

The N- type RESURF layer 25 has a dose of about $5 \times 10^{11}/cm^2$ to $3 \times 10^{12}/cm^2$. The value of specific resistance of the N- type epitaxial layer 24 serving as an elements-formation region is determined based on the characteristics of the transistors Q1 and Q2; it may range from 1 to 20 ohm-cm.

With the aforementioned "double PN junction separation" structure, a total voltage potential of the gate circuit formed in the first region A can be successfully varied within the range from the ground potential (= 0 volts) to the power source voltage Vcc, independently of the gate circuit formed in the second region B. This enables the gate circuits G1 and G2 for controlling and driving a transistor circuit module in Figure 4 to be formed on a "single chip" independently of other circuits. Furthermore, it becomes possible, by properly arranging the impurity dose of the N- type RESURF layer 25, to effectively hold the first region A at a high potential.

A semiconductor device in accordance with the second embodiment of the present invention is generally designated by reference numeral "50" in Figure 5. In this embodiment, a high-voltage MOSFET and its control gate circuitry are integrally formed together using the epitaxial semiconductor wafer in Figure 1.

As in the embodiment in Figure 3, for example, a gate circuit is formed in a first region A using a plurality of transistors separated from each other by PN junction separation. A high-voltage MOSFET is formed in a second region B. The high-voltage MOSFET is formed of a P type base layer 51 serving as a channel layer, an N type source layer 52 formed in the layer 51, a gate electrode layer 54 insulatively disposed above the P type base layer 51 by a gate insulating layer 53, a conductive source electrode layer 55 electrically contacting the source layer 52 and the P type base layer 51, and a conductive drain electrode layer 56 electrically contacting an N+ type diffusion layer 26.

In this embodiment, when the voltage potential of the drain electrode 56 is varied in response to a turn-ON/OFF operation of the MOSFET, a gate circuit formed in the first region A is entirely changed without any influence to the circuitry in circuit operation. Note that this embodiment device may be also fabricated using the manufacturing process described with reference to Figures 2A through 2D.

A semiconductor device 60 in accordance with the third embodiment of the present invention is shown in Figure 6. This embodiment can be considered as an application of the second embodiment. Using the manufacturing process shown in Figures 2A through 2D, a groove 23 is formed in a P- type silicon substrate 21. An N+ type diffusion layer 22 is formed on the inside surface of the groove 23. This groove 23 will be an elements-formation region. By applying an epitaxial growth method and a lapping technique, an N- type semiconductor layer 61 is deposited in the groove 23. An N-type RESURF layer 25 is then formed around this element region in the same manner as in the above-mentioned embodiments. With the wafer, a high-voltage semiconductor element or elements, such as high-voltage MOSFET(s) and/or bipolar transistor(s) can be effectively formed in the N-type layer 61.

Turning to Figure 7, an epitaxial semiconductor

wafer according to the fourth embodiment of the present invention is generally designated by reference numeral "70." A P+ type silicon substrate 21-1 is prepared on which an N- type silicon layer 21-2 is stacked, thereby to constitute an N- type silicon substrate 21. A P-type epitaxial layer 23 is formed on the silicon substrate 21. An N- type epitaxial layer 24 prospectively serving as an elements formation layer is formed on the P- type epitaxial layer 23.

In Figure 7, the substrate surface is divided into three regions A, B, and C, each of which is an elements-formation region in which one or a plurality of elements should be formed. Separating regions D are formed between the elements formation regions A, B, and C. N-type epitaxial layers laid 24 in the elements-formation regions A, B, and C are electrically separated from each other using P+ type diffusing layers 71 by PN junction-separation. These P+ type diffusing layers 71 are formed to have a sufficient depth from the top surface of the wafer to reach the underlying P- type epitaxial layer 23 in the separation regions D.

Of the elements-formation regions, in the first regions A and B, unlike in the second region C, an N+ type semiconductor layer 22 is formed as a first element separation layer and is buried between the P- type epitaxial layer 23 and the substrate 21. N+ type diffusing layers 26 each having a depth from the wafer surface to reach the corresponding N+ type layers 22 are formed around the first regions A and B. The N+ type diffusion layer 26 serve as second element separation layers. An N- type layer 25 shown in Figure 7 is formed outside each of the N+ type layers 26. In the epitaxial wafer 70 of this embodiment, as in the above-mentioned embodiments, each of the element regions A, B, and C has the "N-/P-" type junction separation structure.

A method of manufacturing the epitaxial wafer 70 will be described hereinafter with reference to Figures 8A through 8E, wherein the regions B, C, and D in Figure 7 are illustrated.

As shown in Figure 8A, an N+ type layer 22 having a selected high impurity concentration is formed by diffusion on the top surface of a silicon substrate 21 having a stacked structure consisting of layers 21-1 and 21-2. As shown in Figure 8B, a P- type epitaxial layer 23 is formed on the entire surface of the substrate 21.

Thereafter, as shown in Figure 8C, an N type RESURF layer 25 is formed by ion implantation on the substrate 11 around an elements-formation region in which the N+ type layer 22 is formed, and an N+ type layer 26-1 for surrounding the element region together with the N+ type layer 22 is formed. The N+ type layer 26 is formed to have a depth to reach the N+ type layer 22, thereby defining a layer portion 23 separated by PN junction-separation.

Subsequently, as shown in Figure 8D, an N- type epitaxial layer 24 is grown to cover the entire top surface of the resultant wafer. In the step shown in Figure 8E, a further N+ type layer 26-2 is formed by diffusion to just overlap the N+ type layer 26-1, thereby defining the N- type layer section 24 inside the N+ type layer 26-2. In addition, in order to separate each elements-formation region by PN junction-separation, a P+ type layer 71 is formed by diffusion each separation region between these elements-formation regions. The P+ type layer 71 is formed to have a depth to reach and contact the underlying P- type layer 23.

Attention should be paid to the following point: according to the manufacturing process shown in Figures 8A through 8E, the stacked N+ type diffusing layers 26-1 and 26-2 serving as elements-separation layers together with the n+-type buried layers 22 in the elements-formation regions A and B are respectively formed in two diffusion steps, but these N+ type layers 26-1 and 26-2 can be modified to be formed together in only one diffusion step in the process.

Figures 9A and 9B show the main sectional structures of samples of IC devices obtained by integrally forming a plurality of transistors in elements-formation regions of the epitaxial wafer 70 in Figure 7. In Figures 9A and 9B, two of the plurality of elements-formation regions of the epitaxial wafer 70 are shown: Figure 9A shows a first region B surrounded by an N+ type layer 26; whereas Figure 9B shows a second region C located outside the first region B. One transistor is typically formed in each of the illustrated regions.

An N+ type collector buried layer 41 is formed in each of the regions B and C before an N- type epitaxial layer 24 is formed. (The N+ type collector buried layer 41 is omitted in the embodiment in Figure 7.) In order to separate elements from each other in the regions, a P+ type layer 71 is formed in the second region C simultaneously with formation of a P+ type layer 71 for PN junction-separation from the first region B, and a P+ type layer 72 for separating elements from each other is formed in the first region B. A P type base layer 43, an N type emitter layer 44, and a collector take-out layer 45 are formed in a region surrounded by these layers 71 and 72, as shown in Figure 9A or 9B. It is to be noted that, in these components, suffix "b" (letter "b" comes from region B ) is conveniently added in Figure 9A, while a suffix "c" (letter "c" comes from region C ) is added in Figure 9B for illustrative convenience only.

The transistor circuit in the first region B constitutes a gate circuit G1 shown in Figure 4, for example; the transistor circuit in the second region

C constitutes a gate circuit G2 shown in Fig 4, for instance. In such a case, in the transistor circuit in Figure 9A in the first region B, a terminal P1 for commonly connecting the N+ type layer 26 and the P+ type layer 71 serving as a separation layer for an inner region surrounded by the N+ type layer 26 is used as a reference voltage terminal having a voltage which changes within the range from 0 volts to the power source voltage Vcc. On the other hand, in the transistor circuit in the second region C shown in Figure 9B, a terminal P2 connected to the P+ type separation layer 71 is used as a ground terminal to which a fixed ground potential is applied.

In Figures 9A and 9B, the case wherein NPN transistors are integrally formed has been described above. However, the elements to be formed on the substrate may include other types of elements consisting of gate circuits such as CMOS transistors, diodes, resistors, capacitors, and so forth. When the concentration of an N- type epitaxial layer 14 is set to be a proper value, an N type layer 25 serving as a RESURF layer may be omitted.

In Figure 10, an epitaxial semiconductor wafer in accordance with the fifth embodiment of the present invention is generally designated by reference numeral "100". The wafer 100 differs from the above embodiment shown in Figure 7 in that an N- type epitaxial layer 24 is directly formed on a P- type silicon substrate 21 without forming a P type epitaxial layer. As in the embodiment in Figure 7, a

for separating elements-formation regions A, B, C,... from each other.

In the first region A or B surrounded by N+ type layers 22 and 26, a P- type diffusion layer 101 is formed as an elements formation layer. In the second region C located outside these regions, an N- type layer 24 functions as an elements formation layer. The P-type layer 101 in the first region A or B is subdivided into a plurality of elements-formation sub regions by the N+ type layer 26.

More specifically, in the embodiment in Figure 7 all the elements formation layers are N- type layers, and element separation is performed by P+ type layers. Contrast to this, in the embodiment in Figure 10, elements formation layers include N- and P- types layers of both conductivity types. Therefore, as detailed IC structures will be described later, element separation is performed by a P+ type layer in the N- type layer region; whereas, in the P- type layer region, the element separation is performed by an N+ type.

A method of manufacturing the epitaxial semiconductor wafer 100 will be described below with reference to Figures 11A through 11D. These views of manufacturing steps show a range of the regions B, C, and D.

As shown in Figure 11A, an N+ type layer 22 serving as an elements-separation layer is formed by diffusion on a P- type silicon substrate 21. At this time, the N+ type layer 22 is formed in the region C as needed.

As shown in Figure 11B, an N- type epitaxial layer 24 is then formed on the entire top surface of the resultant substrate. Thereafter, a P+ type layers 71 for separating elements-formation regions from each other is formed by diffusion to have a depth to reach a substrate 21. The elements-formation regions A and B are separated from other regions. An N+ type layer 26 is formed on the elements-formation regions A and B to have a depth to reach the N+ type layer 22, thereby defining a plurality of element regions therein, as shown in Figure 11C. Subsequently, as shown in Figure 11D, P- type layers 101 serving as elements-formation regions are formed by diffusion in the regions A and B.

Samples of IC structures to which the epitaxial wafer 100 of this embodiment is applied are shown in Figures 12 and 13. Figure 12 shows a partial wafer structure according to the first region A (or B), whereas Figure 13 shows a partial wafer structure according to the second region C.

As shown in Figure 12, a plurality of elements-formation regions formed in the first region A are separated by the N+ type layers 26 from each other. In these separated regions, NPN transistors, PNP transistors, CMOS transistor circuits, and re- [illegible] integrally formed. In Figure 12, reference letters "PNP", "NPN", "CMOS", and "R" are respectively added to these components for the sake of easy identification. In the IC structure, unlike the embodiment in Figure 10, the P- type layer 101 serving as an elements formation layer is formed to have a depth to reach the underlying N+ type layer 22. The resistor R is constituted by an N- type layer formed by diffusion on the P- type layer 101. The CMOS circuit is constituted by forming a P-channel MOSFET and an N-channel MOSFET in an N type well region and a P type well region formed in the P-type layer 101. An NPN transistor is a lateral transistor obtained by forming an emitter and a collector by diffusion and using the P- type layer 101 as a base of the NPN transistor. A PNP transistor is constituted by defining a conventional planar structure using the P-type layer 101 as a collector layer of the PNP transistor.

A plurality of element regions in the second region C are separated from each other by P+ type layers 71 as shown in Figure 13. As in the above embodiment in Figure 12, an NPN transistor, a PNP transistor, a CMOS transistor circuit, and a resistor R are integrally formed in each of the separated regions. A conductivity type of elements

formation layers in the second region C is opposite to that in the first region A in the region C. With the above description, the resistor R in Figure 13 is formed by a P type diffusion layer. The CMOS circuit is formed in the N type well region and the P type well region, as in the region A. Structures of the PNP transistor and the NPN transistor in the region C are opposite to those in the above region A; the PNP transistor has a lateral structure, and the NPN transistor has a planar structure.

A transistor circuit formed in the region A of each of the wafers shown in Figure 12 and 13 is a gate circuit on a high voltage side, as in the previously presented embodiments; and a transistor formed in the region C is used as a gate circuit on a low voltage side. The N+ type layer 26 in Figure 12 is set to be the maximum voltage potential, and the N+ type layer 71 is set to be the minimum voltage potential, i.e., a normal ground potential (= typically 0 volts). With the above potential setting, PN junction separation between the high and low voltage sides of this circuitry can be further confirmed. By employing the "double PN junction separation", as in the above-mentioned embodiments, the reference voltage of the transistor circuit in the region A in Figure 12 can be desirably changed within the range between the ground potential (0 volts) and the power source voltage Vcc, independently of the reference voltage of the transistor circuit in the region C in Figure 12. Using the IC structure, gate circuits G1 to G6 for driving/controlling the transistor circuit module shown in Figure 4 can be effectively packaged in one chip.

It should be noted in Figure 12 that the P- type layer 101 is not always absolutely required, and, for example, the P- type layer 101 need not be formed in a region for forming a resistor. Similarly, in the wafer structure in Figure 13, N+ type buried layers 22 in a PNP transistor-formation region or a CMOS circuit-formation region can be omitted depending on conditions.

## Claims

1. A substrate structure (20, 50, 60, 70, 100) comprising a semiconductive substrate (21) having a PN junction layer (24), characterized in that a closed region (A) is formed on said substrate (21) to be separated by PN junction from the remaining portions of said substrate (21), said closed region (A) having a PN junction layer (24) structurally equivalent to said PN junction layer (24) of said substrate (21).

2. The device as recited in claim 1, characterized by further comprising semiconductive separation layer means (22, 26), formed in said substrate (21) to define said closed region (A), for electrically separating said region from the remaining portions of said substrate (21).

3. The device as recited in claim 2, characterized in that said closed region (A) serves as an elements-formation region for allowing formation of a semiconductor active element (Q1) PN junction-separated inside said region (A).

4. The device as recited in claim 3, characterized in that said semiconductor active element includes a high-voltage transistor (Q1).

5. The device as recited in claim 4, characterized in that said high-voltage transistor (Q1) is one of a unipolar transistor and a bipolar transistor.

6. The device as recited in claim 3, characterized by further comprising a lightly-doped semiconductive layer (25) formed in said substrate (21) to surround said elements-formation region (A), having the same conductivity type as that of said separation layer means (22, 26), and serving as a reduced surface filed layer.

7. A semiconductor device (20, 50, 60, 70, 100) comprising a wafer layer (21) of a first conductivity type, and a heavily-doped semiconductive separation layer (22, 26) of a second conductivity type formed on said wafer layer (21) to define a first closed region (A) and a second region (B) adjacent to the first region, characterized in that said device further comprises a PN junction structure provided in said first region (A) and having a semiconductive layer (23) of the first conductivity type and a lightly-doped semiconductive layer (24) of the second conductivity type stacked on said semiconductive layer (24) and serving as a first elements-formation layer, a lightly-doped semiconductive layer (24) of the second conductivity type formed on said wafer layer (21) in the second region and serving as a second elements-formation layer, and a semiconductor element (Q1) formed in said first elements-formation layer to be separated by PN junction, thereby to provide a double PN junction separation structure in which said first region (A) is separated by PN junction from said second region (B) and said semiconductor element (Q1) is separated by PN junction in said first region (A).

8. The device as recited in claim 7, characterized in that said first elements-formation layer (24) is substantially equal in thickness to said second elements-formation layer (24).

9. The device as recited in claim 8, characterized by further comprising a lightly-doped semiconductive layer (25) formed on said wafer layer (21) to surround said heavily-doped semiconductive separation layer (22, 26) and serving as a reduced surface field layer layer called a RESURF layer.

10. The device as recited in claim 8, characterized in that said semiconductor element includes a high-voltage transistor.

11. The device as recited in claim 10, characterized by further comprising a second semiconductor element (Q2) formed in said second elements-formation layer (24), said second semiconductor element including a high-voltage transistor.

12. The device as recited in claim 8, characterized in that the stacked layers (23, 24) of said PN junction structure include an epitaxial layer.

13. The device as recited in claim 8, characterized in that the stacked layers (23, 24) of said PN junction structure are epitaxial layers.

14. The device as recited in claim 8, characterized in that the stacked layers (23, 24) of said PN junction structure include a diffusion layer.

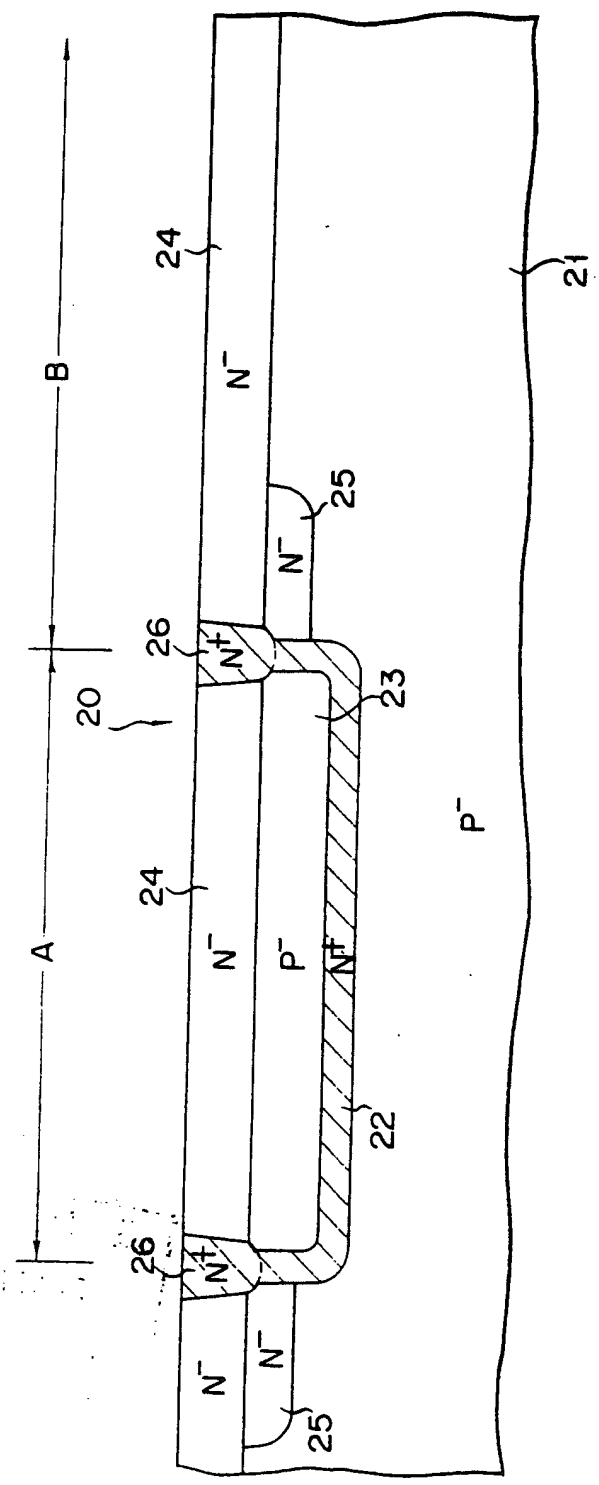


FIG. 1

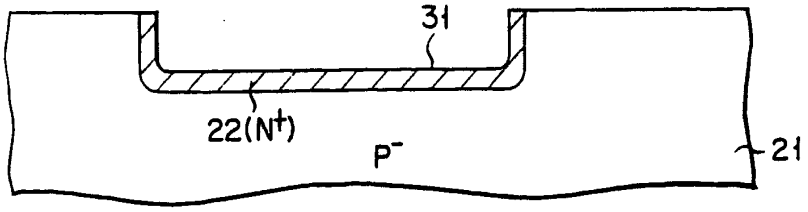


FIG. 2A

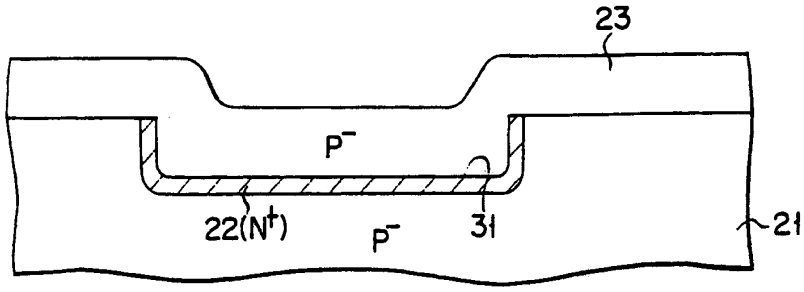


FIG. 2B

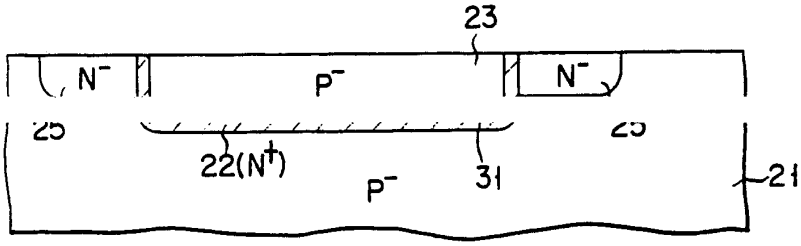


FIG. 2C

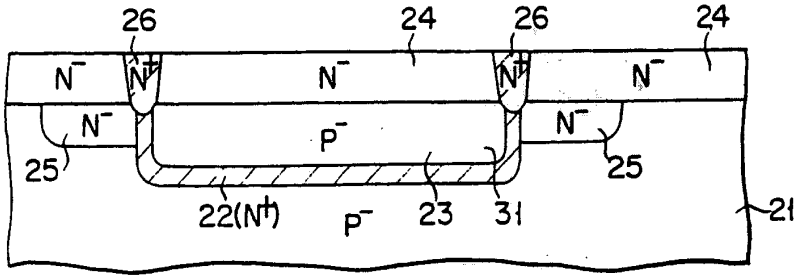


FIG. 2D

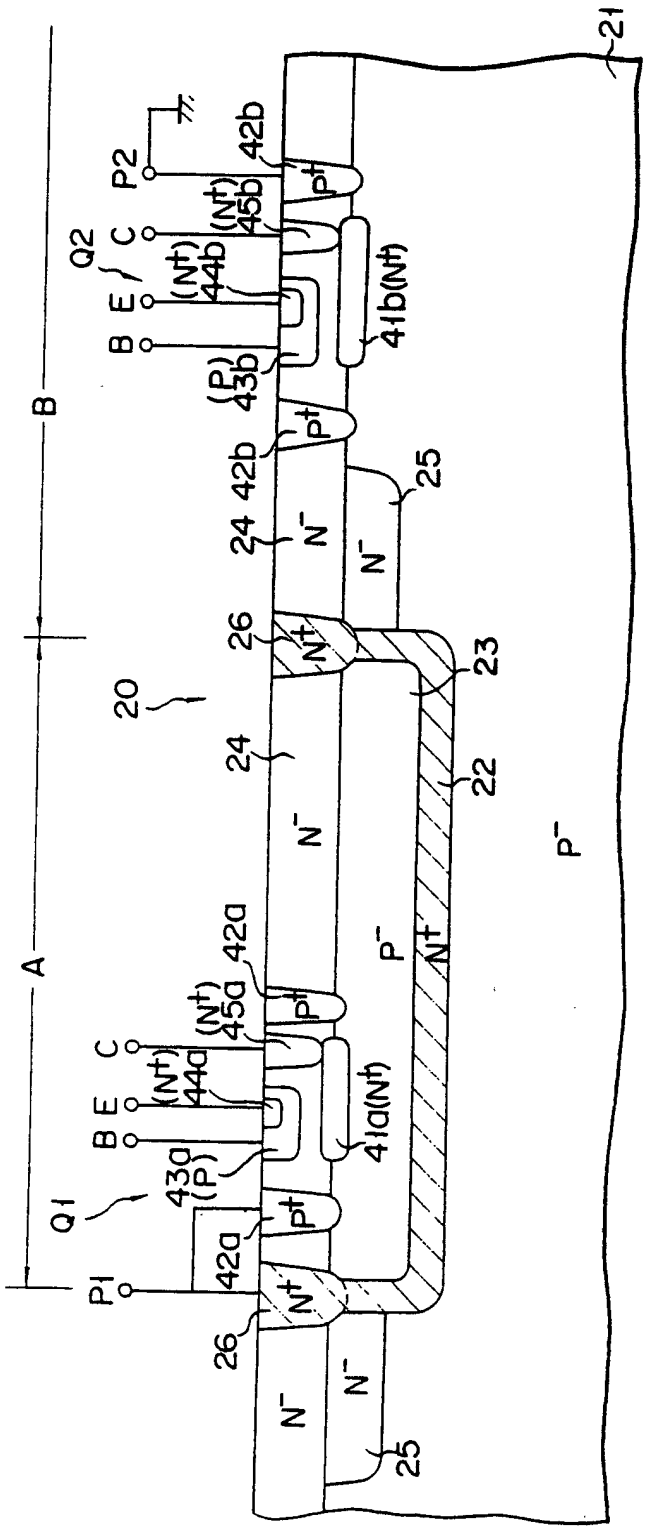
21
P2
42b
(N+)
45b
C
Q2
(N+)
44b
B
E
B
41b(N+)
(P)
43b
P+
42b
25
24
N-
N-
26
N+
23
20
24
22
N-
P-
P-
N+
42a
(N+)
45a
C
(N+)
44a
B
E
41a(N+)
43a
(P)
Q1
P+
42a
P1
N+
26
N-
N-
25
A
B

FIG. 3

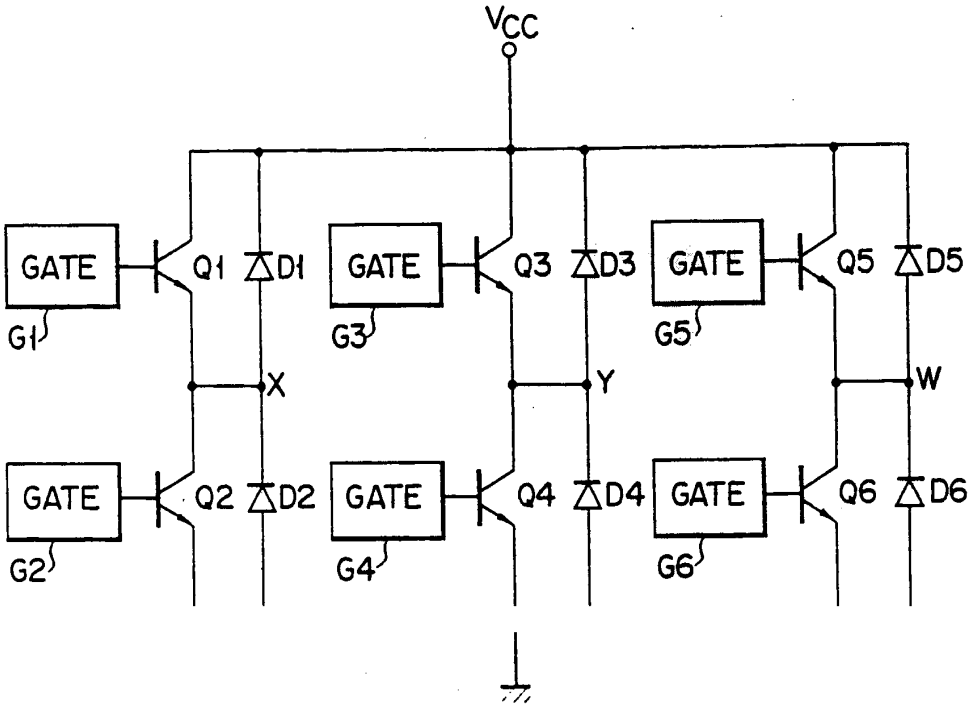
VCC
GATE
Q1
D1
G1
GATE
Q3
D3
G3
GATE
Q5
D5
G5
X
Y
W
GATE
Q2
D2
G2
GATE
Q4
D4
G4
GATE
Q6
D6
G6

FIG. 4

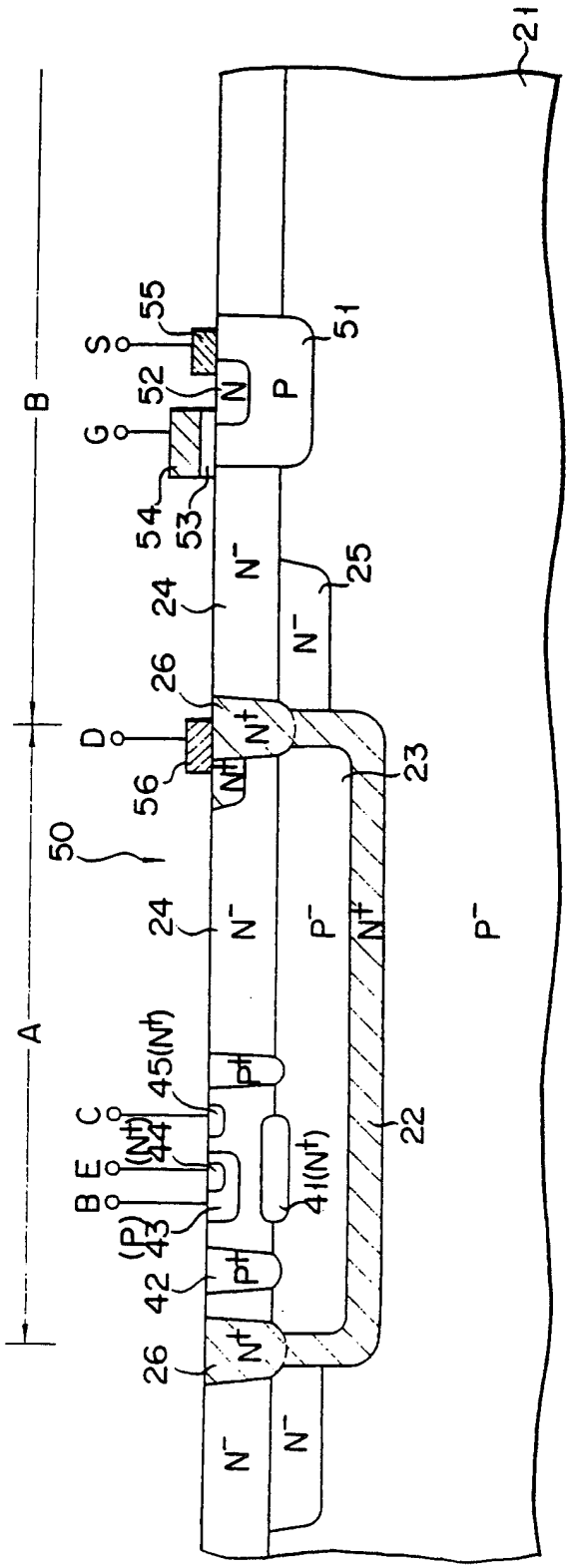
21
S
55
52
N
P
51
G
54
53
N⁻
25
24
N⁻
26
D
N⁺
56
(N⁺)
23
50
24
N⁻
P⁻
N⁺
P⁻
A
B
45(N⁺)
P⁺
C
(N⁺)
44
B
E
(P)
43
41(N⁺)
22
42
P⁺
26
N⁺
N⁻
N⁻

FIG. 5

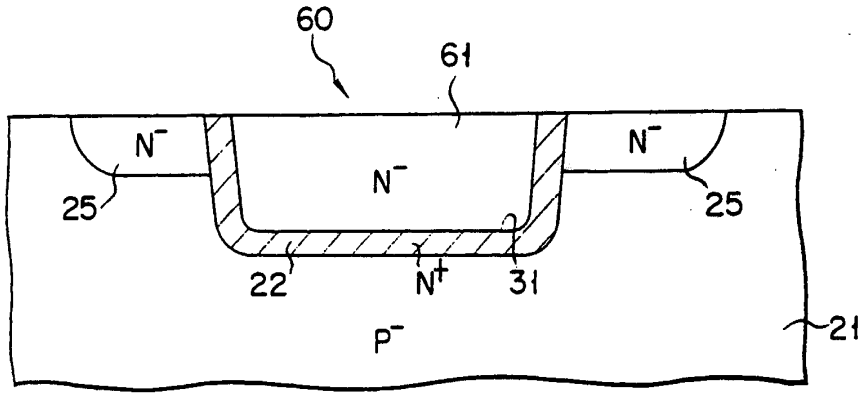


FIG. 6

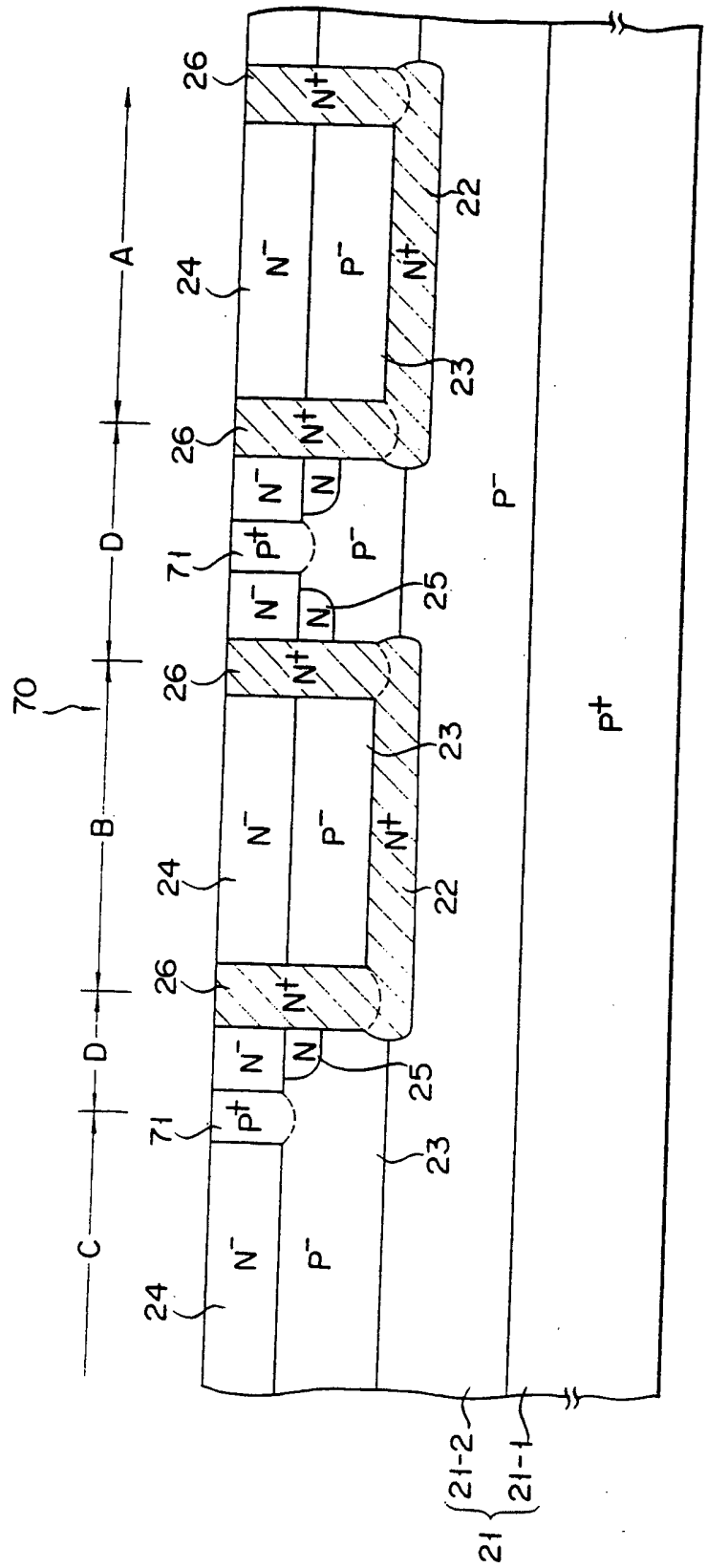


FIG. 7

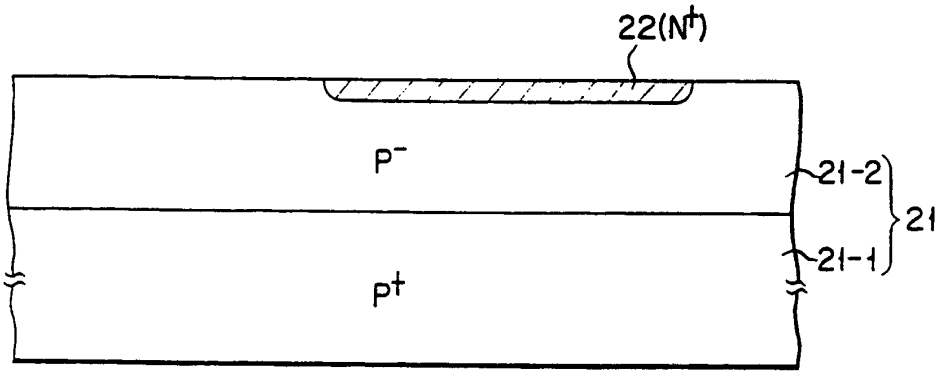


FIG. 8A

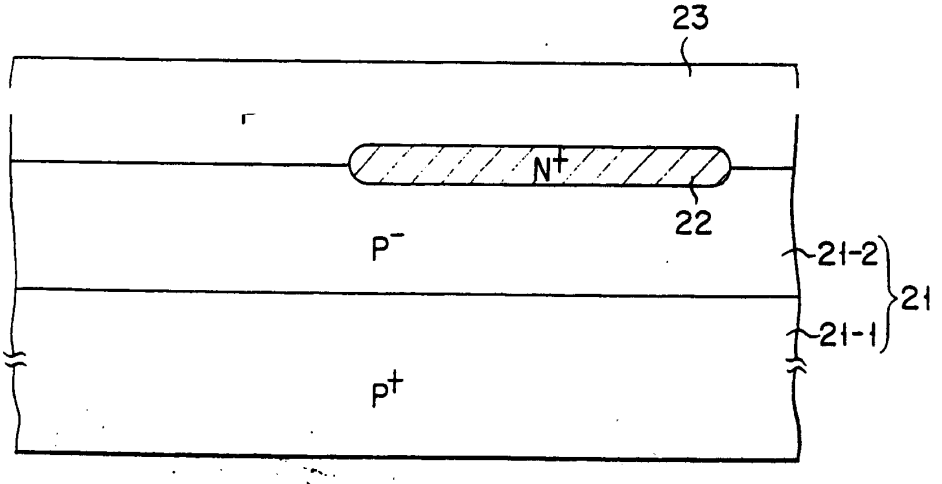


FIG. 8B

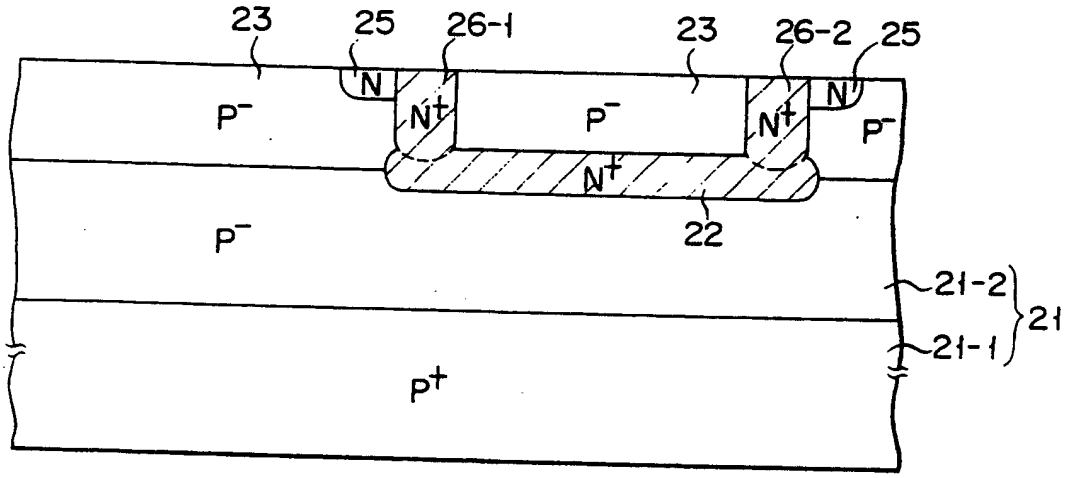
23
25
26-1
23
26-2
25
N
N+
P-
P-
N+
N+
P-
P-
22
21-2
21
21-1
P+

FIG. 8C

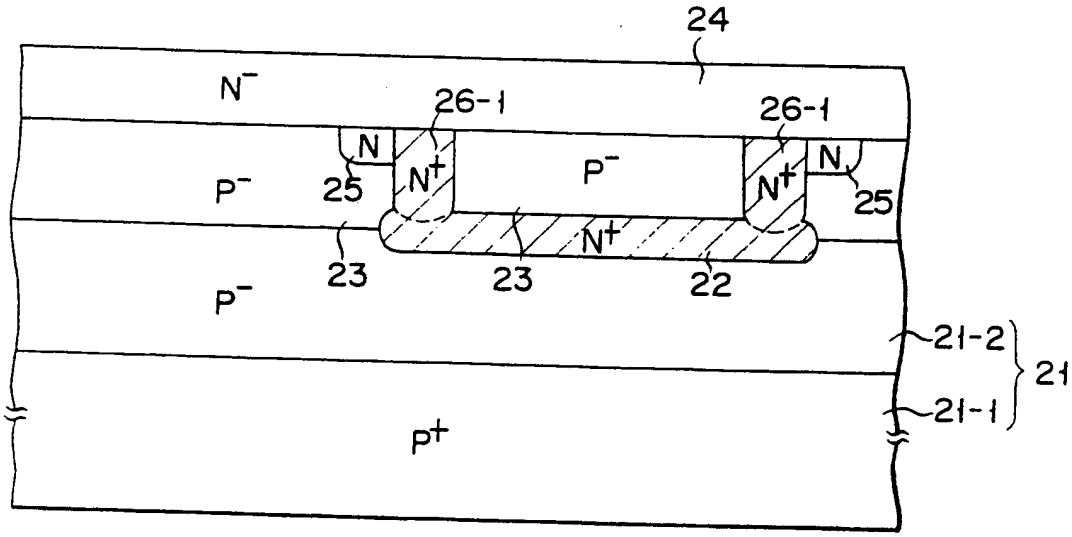
24
N-
26-1
26-1
N
N+
P-
N+
N
P-
25
25
N+
23
23
22
P-
21-2
21
21-1
P+

FIG. 8D

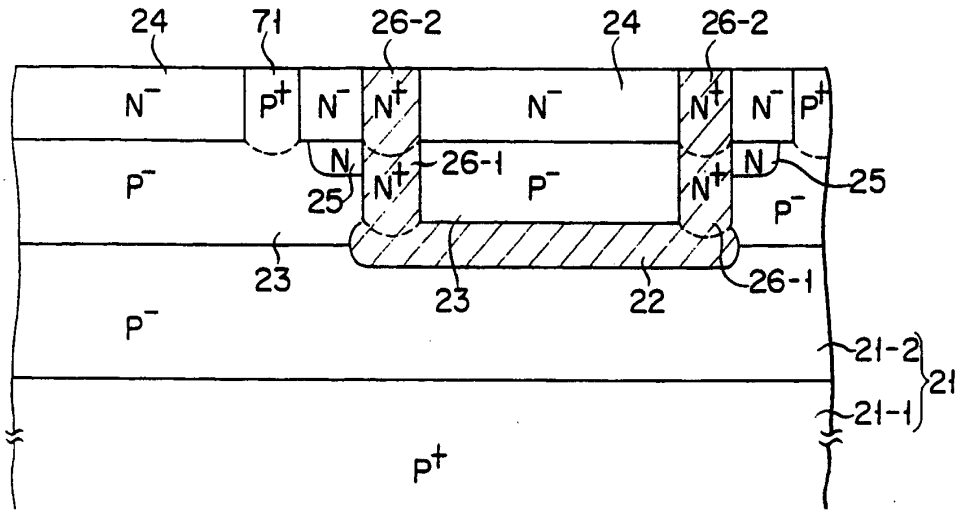
24
71
26-2
24
26-2
N⁻
P⁺
N⁻
N⁺
N⁻
N⁺
N⁻
P⁺
N
N⁺
26-1
N
N⁺
N
25
25
P⁻
P⁻
P⁻
P⁻
23
23
22
26-1
21-2
21
21-1
P⁺

FIG. 8E

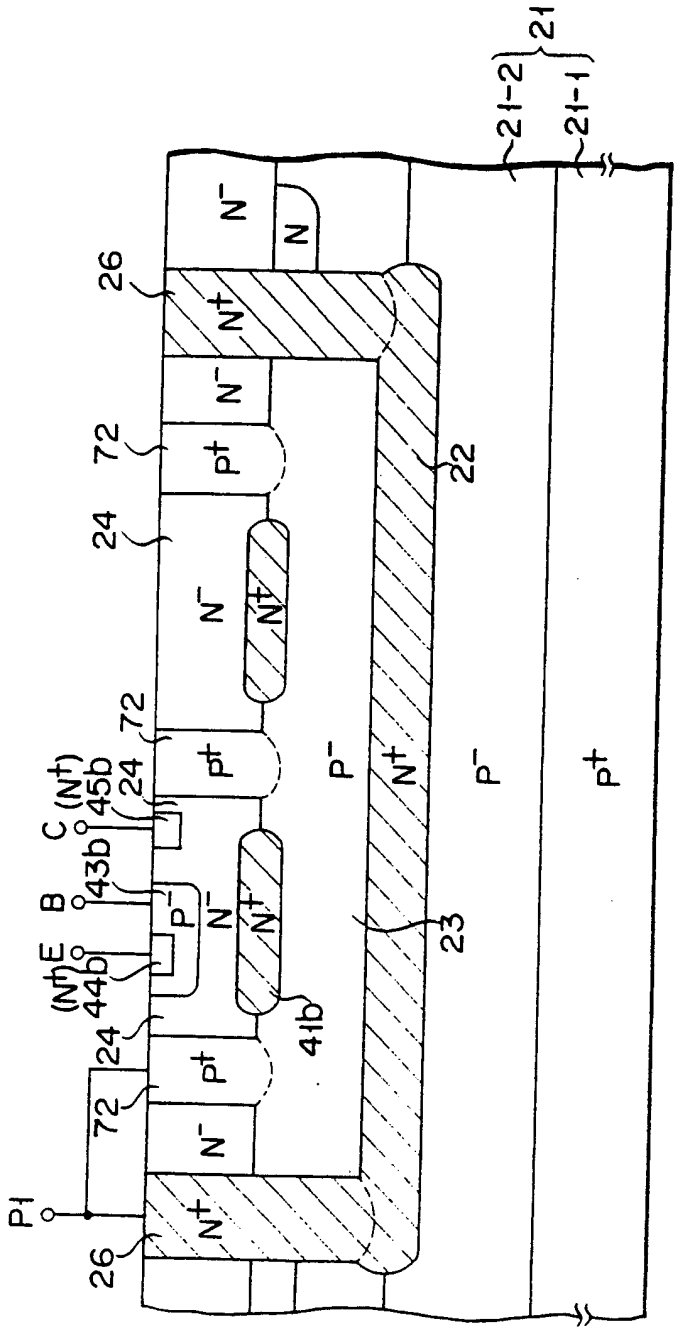
21
21-2
21-1
N⁻
N
N⁺
26
72
P⁺
22
24
N⁻
N⁺
72
P⁺
C (N⁺)
45b
24
B
43b
E
(N⁺)
44b
P⁻
N⁻
N⁺
23
41b
24
72
P⁺
N⁻
N⁺
P1
26
P⁻
N⁺
P⁻
P⁺

FIG. 9A

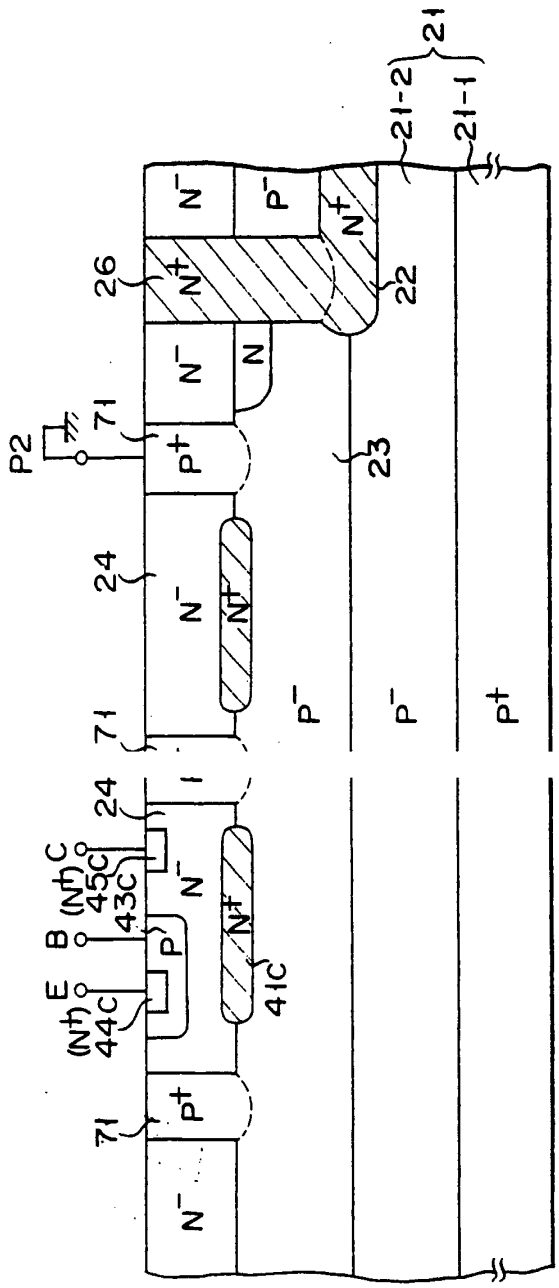
21
21-2
21-1
N⁻
P⁻
N⁺
22
26
N⁺
N⁻
N
71
P2
P⁺
23
24
N⁻
N⁺
71
P⁻
P⁻
P⁺
24
C
(N⁺) 45C
43C
B
N⁻
P⁺
N⁺
41C
E
(N⁺) 44C
71
P⁺
N⁻

FIG. 9B

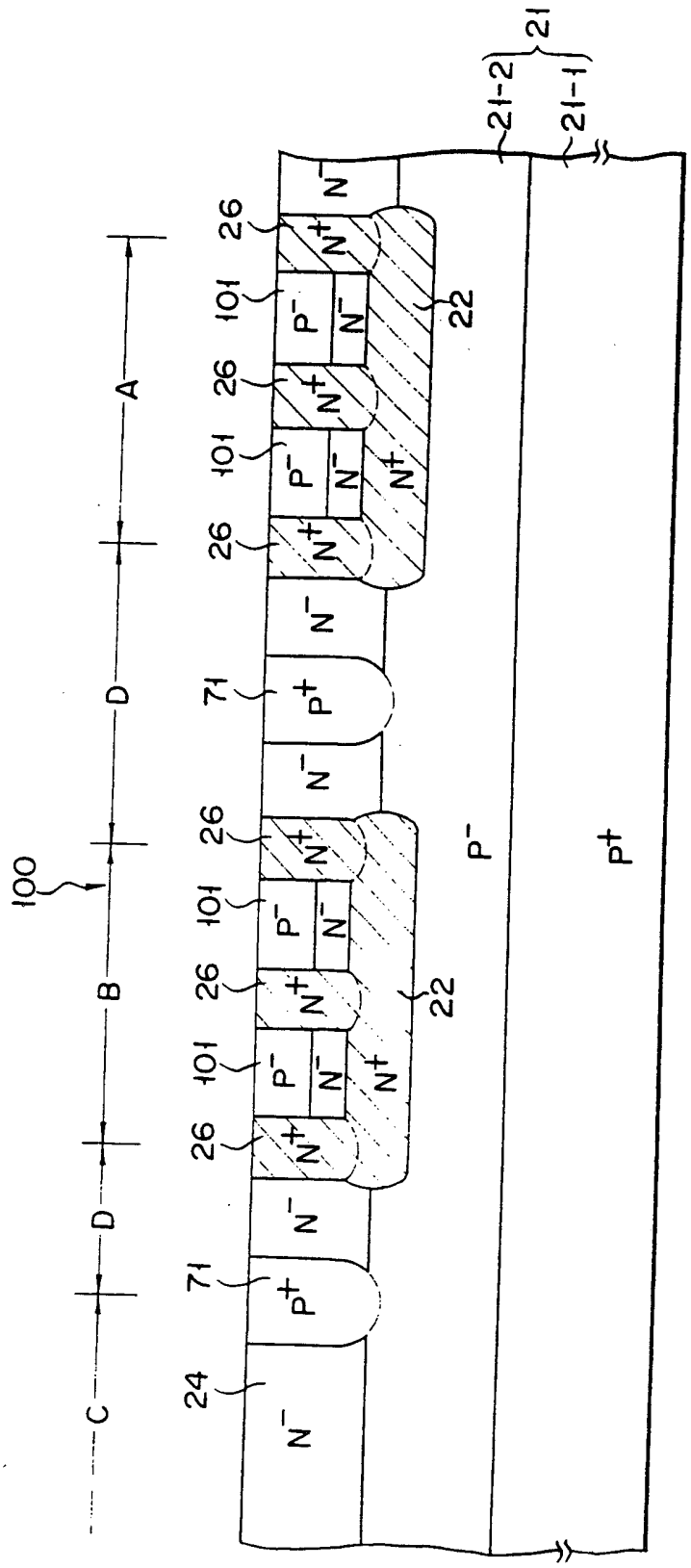


FIG. 10

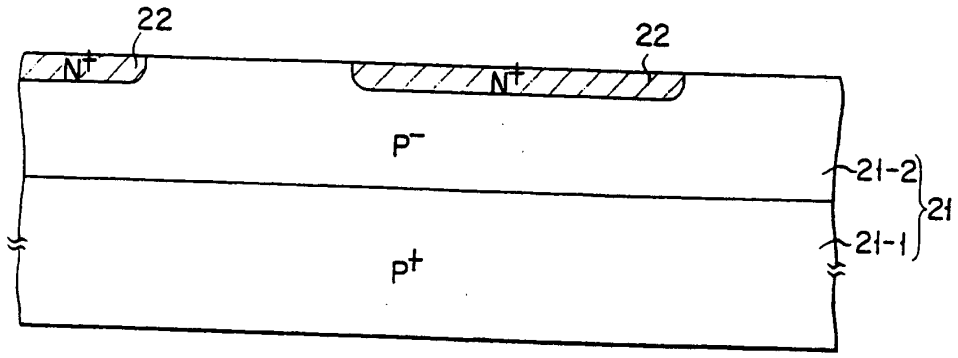


FIG. 11A

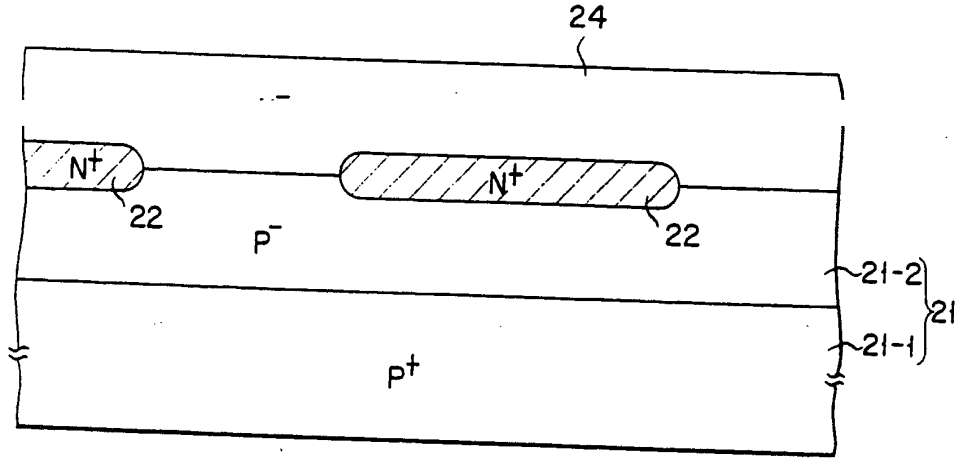


FIG. 11B

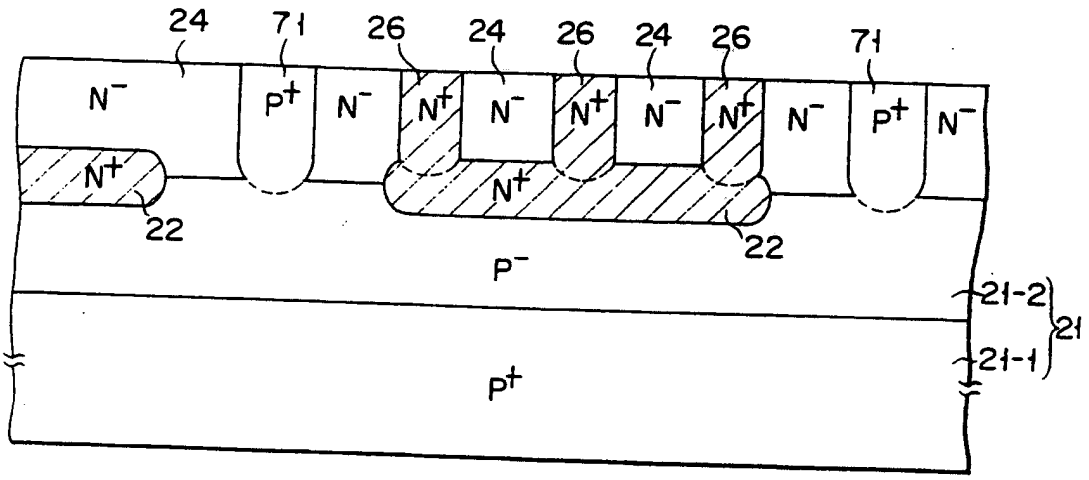


FIG. 11C

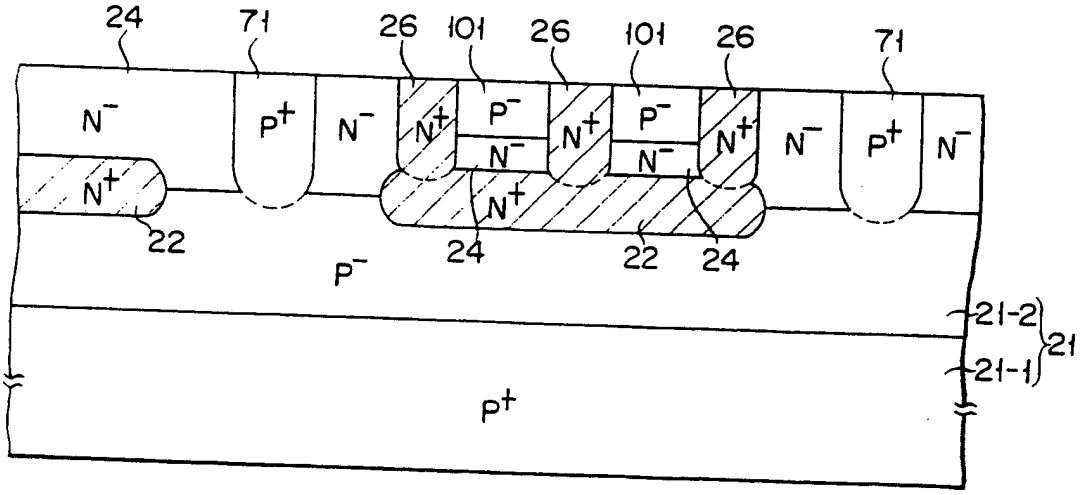


FIG. 11D

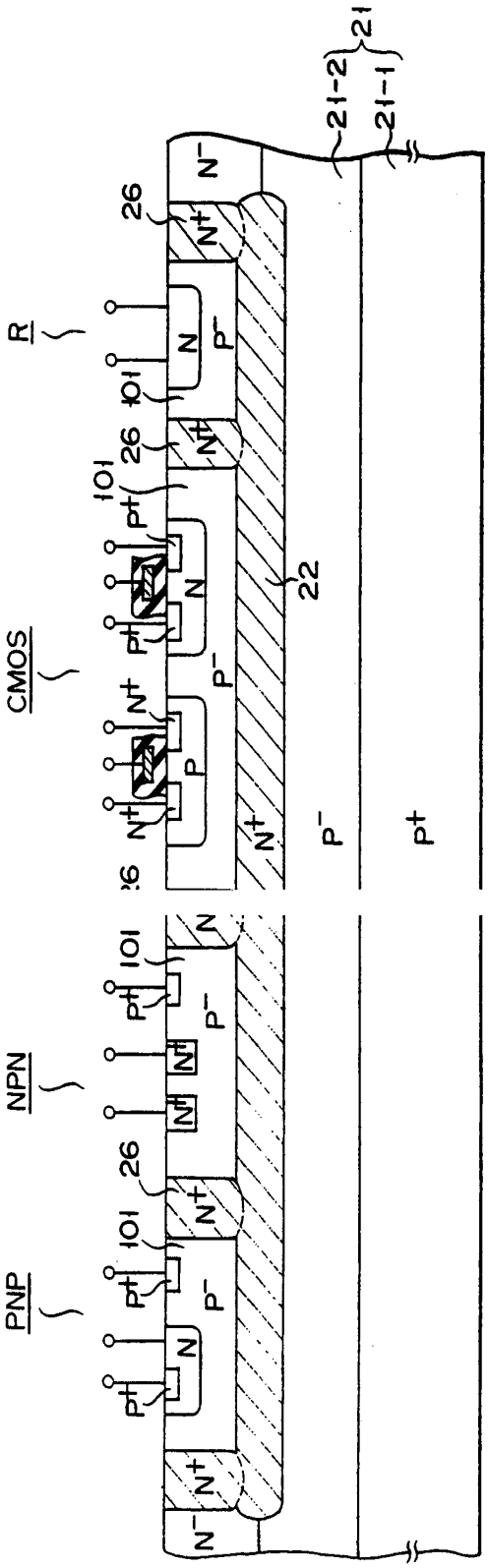


FIG. 12

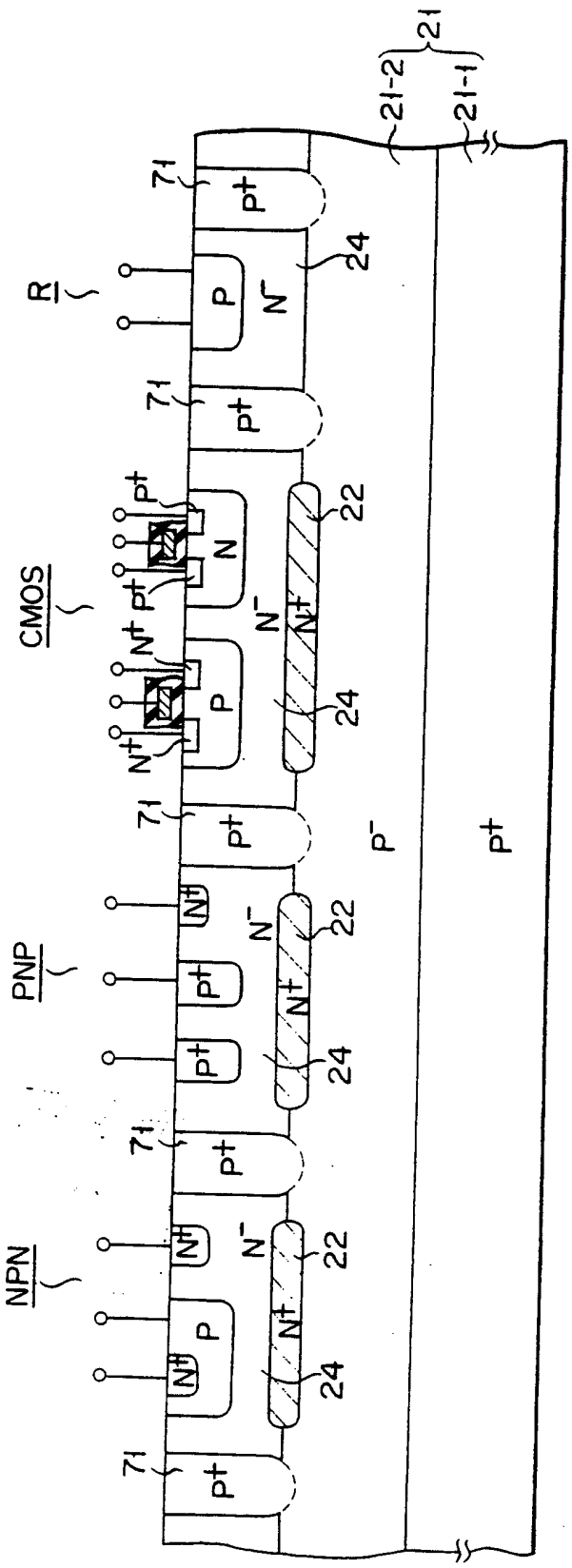


FIG. 13

European Patent Office

# EUROPEAN SEARCH REPORT

Application Number

EP 90 31 0645

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int. Cl.5) |
|---|---|---|---|
| A | GB-A-2 175 138 (SGS MICROELETTRONICA)<br>* Figure 5 * | 1-5,7, 11-14 | H 01 L 21/76 |
| A | FR-A-2 154 786 (SONY)<br>* Figure 6 * | 1-5,7, 11-14 | |
| A | EP-A-0 117 867 (MITSUBISHI)<br>* Figure 2 * | 1 | |
| A | FR-A-2 309 040 (TOSHIBA)<br>* Figure 2 * | 1 | |
| A | EP-A-0 156 964 (MOTOROLA)<br>* Figures 3A-3AG * | 5 | |
| A | IEDM 1984, San Francisco, 9th - 12th December 1984, pages 698-701, IEDM; T. OKABE et al.: "180V Analog-compatible high-speed logic utilizing semi-well isolation technology"<br>* Figure 1 * | 7,8,10-14 | |
| A | L'ONDE ELECTRIQUE, vol. 67, no. 6, November 1987, pages 58-69, Paris, FR; P. ROSSEL: "M.O.S. technologies for smart power and high-voltage circuits"<br>* Figure 7 * | 6,9 | TECHNICAL FIELDS SEARCHED (Int. Cl.5)<br>H 01 L 21/76 |

The present search report has been drawn up for all claims

| Place of search | Date of completion of search | Examiner |
|---|---|---|
| The Hague | 17 December 90 | VANCRAEYNEST F.H. |

CATEGORY OF CITED DOCUMENTS

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D: document cited in the application
L: document cited for other reasons

&: member of the same patent family, corresponding document

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APPLICANT: Werner

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